REMARKS

Applicant appreciates the examination evidenced by the Final Official Action mailed May 31, 2002 (hereinafter the Final Official Action). Applicant maintains that Sato does not disclose "forming a dielectric layer on an integrated circuit substrate, the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer" as discussed in Applicant's response dated April 5, 2002. In particular, Figures 3, 8, and 11 of Sato relied on in the Final Official Action appear to show a conductive layer with conductive material formed in grooves therein. Respectfully, Applicant submits that these figures show a dielectric layer, not a conductive layer, although it is not clear to Applicant why the Final Official Action is interpreting Sato's figures in this way, as Sato clearly describes layer 100 as a conductor. *See, for example, Sato, col. 4, lines 54-56, describing upper and lower* ***electrode*** *layers 100, 110.*

However, in order to further advance prosecution of the application, Applicant has amended independent Claim 35 to recite in-part:

> forming a dielectric layer **having first and second opposing faces** on an integrated circuit substrate, the dielectric layer including a closed via therein **that extends from the first face to the second face and** that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer; and
>
> forming a conductive pattern **that extends from the first face to the second face** in the closed via and on the dielectric layer opposite the substrate,

recitations that are not disclosed or suggested by the cited art (independent Claim 40 has been similarly amended). Claim 40 has been similarly amended.

The Final Official Action appears to consider the grooves shown in Figure 8 of Sato to disclose the "via therein that encloses..." recited in the claims. Even if this were true, the grooves in Sato do not extend from the first face to the second face of the dielectric layer as recited in the amended claims. Accordingly, Sato does not disclose or suggest the recitations of Claims 35 and 40.

Applicant submits that independent Claims 35 and 40 are patentable for at least the reasons discussed herein. Furthermore, dependent Claims 36-39 and 41 are

patentable at least per the patentability of the amended independent claims. Applicant, therefore, respectfully requests favorable examination of the application and the allowance of all claims. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919)854-1400.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box RCE, Commissioner for Patents, Washington, DC 20231, on August 13, 2002.

Audra Wooten
Date of Signature: August 13, 2002

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Sir:

The following is an addendum to the concurrently filed amendment in response to the Final Official Action of May 31, 2002 in the above referenced application. This addendum includes a marked-up version of the changes made to the claims by the present amendment.

In the Claims:

Claims 35 and 40 have been amended as follows:

35. (Amended) A method of forming a bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer having first and second opposing faces on an integrated circuit substrate, the dielectric layer including a closed via therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer; and

forming a conductive pattern that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate.

40. (Amended) A method of forming a bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer having first and second opposing faces on an integrated circuit substrate, the dielectric layer including a closed via therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer, wherein the closed via penetrates the dielectric layer and extends towards the integrated circuit substrate; and

forming a conductive pattern that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate.

END